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LOS ANGELES, CALIFORNIA 90064-1683

(310) 312-2000  
FAX: (310) 312-3100

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E-MAIL ADDRESS ses@msk.com

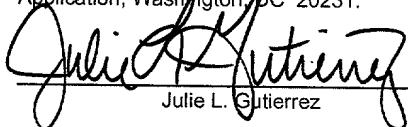
STEVEN E. SHAPIRO  
PROFESSIONAL CORPORATION  
TELEPHONE: (310) 312-3112  
FAX: (310) 312-3786

June 24, 1999

"Express Mail" Receipt No. AB13164491X

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I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Box Patent Application, Washington, DC 20231.

  
Julie L. Gutierrez

Commissioner of Patents and Trademarks  
Box Patent Application  
Washington, DC 20231

**Subject: Transmittal of Application for United States Letters Patent**  
Attorney Docket No.: 30454-230 (P-3376)

Dear Sir:

Transmitted herewith for filing is the patent application of:

Inventor: William Eric Corr

Entitled: DETERMINING TIMING OF INTEGRATED CIRCUITS

The filing fee has been calculated as shown below:

	No. Filed	No. Extra	Small Entity		Other Than Small Entity	
Basic Fee				\$380.00		\$760.00
Total Claims	12 - 20 =	0	x \$9=		x \$18=	
Ind. Claims	2 - 3 =	0	x \$39=		x \$78=	
2 Multiple Dependent Claims		0+ \$130=		+ \$260=	260.00	
TOTAL						\$1,020.00

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Commissioner of Patents and Trademarks  
June 24, 1999  
Page 2

Enclosed are the following:

1. 11 pages of specification, claims and abstract;
2. 4 pages of informal drawings;
3. Unsigned Declaration and Power of Attorney;
4. Check in the amount of \$1,020.00 to cover filing fees; and
5. Preliminary Amendment.

The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 13-3735. A duplicate copy of this sheet is enclosed.

Any additional filing fees required under 37 C.F.R. 1.16.  
 Any patent application processing fees under 37 C.F.R. 1.17.

It is respectfully requested that the Commissioner accord the enclosed patent application a filing date and serial number.

Respectfully submitted,

MITCHELL, SILBERBERG & KNUPP LLP

By

Steven E. Shapiro  
Registration No. 35,676

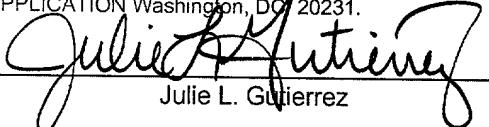
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Julie L. Gutierrez

**PATENT**

Atty. Docket No. 30454-00230

P-3376

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of:

WILLIAM ERIC CORR

Serial No.: To be Assigned

Filed: Herewith

For: DETERMINING TIMING OF  
INTEGRATED CIRCUITS

Group Art Unit: Unknown

Examiner: Unknown

**PRELIMINARY AMENDMENT**

Box PATENT APPLICATION  
Commissioner of Patents and Trademarks  
Washington, DC 20231

Sir:

Prior to the examination of the above-referenced patent application being filed herewith, please amend the application as follows:

**IN THE CLAIMS:**

Please amend the claims as follows:

7. (Amended) A method according to [any of claims 3 to 6,] to claim 3, wherein the effects of aggressor wire in any category are scaled according to their respective topological coupling and respective electrical signal coupling with the victim wire.

### REMARKS

The amendment to claim 7 removes the multiple dependency form of the claim and no new matter is added by the amendment.

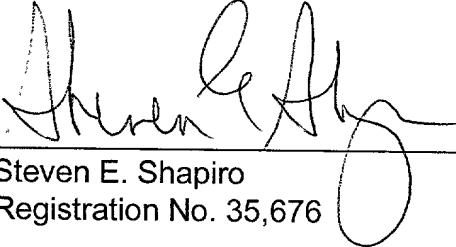
### CONCLUSION

It is not believed that any fees are due in connection with the filing of this paper. However, if there are any fees due, the Commissioner is hereby authorized to charge such fees to our Deposit Account No. 13-3735. A duplicate copy of this page is attached for that purpose.

Respectfully submitted,

**MITCHELL, SILBERBERG & KNUPP LLP**

By \_\_\_\_\_



Steven E. Shapiro  
Registration No. 35,676

Dated: June 24, 1999

**MITCHELL, SILBERBERG & KNUPP LLP**  
11377 West Olympic Boulevard  
Los Angeles, California 90064  
Telephone: (310) 312-2000  
Facsimile: (310) 312-3100

# UNITED STATES APPLICATION FOR LETTERS PATENT

for

## DETERMINING TIMING OF INTEGRATED CIRCUITS

by

**William Eric Corr**

12 Knowe Road  
Twickenham, Mid, England TW2-6QH  
United Kingdom  
Citizenship: British

"Express Mail" Receipt No. AB13164491X

Date of Deposit June 24, 1999

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Julie L. Gutierrez

## DETERMINING TIMING OF INTEGRATED CIRCUITS

The present invention relates to a method and means for determining timings of operation of the various elements in a synchronous integrated circuit.

Static timing analysis tools are usually constructed as program that runs on a computer system which reads and writes information from a database which contains information on the logical and physical construction of an integrated circuit. This type of program is typically referred to as a "design tool".

Conventional static timing analysis tools determine whether storage devices will work reliably by looking at the predicted timing delays between their clock and data pins switching. If the difference in time between the signal switching at the pins is smaller than the device can tolerate, it may become "metastable", that is its output becomes indeterminate which would cause problems for other circuit elements and unreliable system operation.

The disadvantage of such tools is that they assume that all signal propagate around the die of an integrated circuit with a speed that is governed only by the dimensions of the wire and the strength of the driving element. Unfortunately, in complex integrated circuits this is not strictly true. Many wires cross or run parallel to each signal wire, and any switching activity in these wires may perturb the flight time of a signal in the victim wire. This effect is known as "crosstalk" and is a dynamic effect. It depends on switching activity. Conventional timing analysis is static, it does not require any switching information to determine whether or not the integrated storage elements will work reliably. Thus, it is open to making incorrect assumptions about the time signals take to travel around the chip and will not reliably predict which paths really are likely to cause timing problems.

## SUMMARY OF THE INVENTION

It is an object of the invention to provide a method and means for improving the operation of synchronous integrated circuits and alleviating the effects of dynamic crosstalk.

In the first aspect, the present invention provides a method of determining the timing for a synchronous integrated circuit, the circuit including a multiplicity of clocked elements interconnected by signal paths, the method comprising:

- 1) forming predictions for timing delays in said signal paths in the integrated circuit;
- 2) selecting a first such path, tracing wires in the integrated circuit forming the path (hereinafter referred to as victim wires) and determining adjacent and crossing wires thereto (hereinafter referred to as aggressor wires);
- 3) for each aggressor wire, determining the amount of perturbation coupling to the victim wires of the first path;
- 4) dividing the aggressor wires into a plurality of categories depending on the clocked timing of the aggressor wires in relation to the clocked timing of the victim wires;
- 5) adding margins of error to the clocked timing of the victim wires in dependence upon the number of aggressor wires in one or more of said categories.

In a second aspect, the present invention provides apparatus for determining the timing of a synchronous integrated circuit, the circuit including a multiplicity of clocked elements interconnected by signal paths, the apparatus comprising:

- 1) means for forming predictions for timing delays in said signal paths in the integrated circuit;
- 2) means for selecting a first such path, tracing wires in the integrated circuit forming the path (hereinafter referred to as victim wires) and determining adjacent and crossing wires thereto (hereinafter referred to as aggressor wires);

- 3) means for determining the amount of coupling, for each aggressor wire, to the victim wires of the first path;
- 4) means for dividing the aggressor wires into a plurality of categories depending on the clocked timing of the aggressor wires in relation to the clocked timing of the victim wires;
- 5) means for adding margins of error to the clocked timing of the victim wires in dependence upon the number of aggressor wires in one or more of said categories.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

A preferred embodiment of the invention will now be described with reference to the accompanying drawings wherein:

Figure 1 is a commonly used timing diagram for a clocked element for a known method of static timing analysis;

Figure 2 is a conceptual diagram of aggressor wires or nets crossing a victim wire or net, in accordance with the invention;

Figure 3 is a conceptual timing diagram similar to figure 1 but with additional margins added for the clocked timing relationship in accordance with the present invention; and

Figures 4, 5 and 6 are flow-charts of the method in accordance with the invention.

#### **DESCRIPTION OF THE PREFERRED EMBODIMENT**

Referring to figure 1, a clocked element 2, e.g. a flip-flop, has a data line 4 and a clock line 6.

As is usual, if data is to be applied on line 4 to the element 2, the data is presented on line 4 well before the occurrence of the clock signal on line 6 in order to ensure that variations in timing do not cause incorrect operation. As can be seen, there is to the left of the rising edge of the clock pulse a time margin based on the set-up time for the circuit, and a time margin to the right of the rising edge of the clock pulse known as the hold time critical region in which operation of element 2 should take place with

data present on line 4 and a clock pulse on line 6. Data should be present on line 6 throughout this period.

The apparatus in accordance with the invention, or "tool" operates in several phases, looking at all parts in an integrated circuit which include elements such as that shown in figure 1, and the time it takes for signals to travel from one pin of one element to the next.

In accordance with the invention, the topological nature of each signal path is examined, as indicated in figure 2, wherein the signal path comprises a wire between components 10, 12, each wire being referred to as victim wire, and the combination of victim wires being referred to as a victim net 14. The victim net is examined, looking at the number of "aggressor wires" 16 crossing and/or running parallel to the victim net to determine the amount of perturbation clocked signals in the aggressor wires would have on the victim net, should the aggressor wires switch at exactly the same time as a signal being transmitted in the victim net.

The actual amount of perturbation (a static timing analysis) is calculated based on the following criteria:

- 1) Topology of the coupling, i.e. are the wires crossing or in parallel
- 2) The layer in the semiconductor chip that the wires are on
- 3) The strength or power of the drivers in the victim and aggressor nets
- 4) The operating conditions such as process, voltage and temperature
- 5) The nature of the wire - static/power supply/dynamic

Static wires would have no effect so can be discounted from the list. Dynamic wires do have an effect so must be analysed, in terms of their switching in relation to the victim wire. Power supply wires may have an effect. This is hard to quantify due to the complex nature of the switching of the cells attached to the power nets, so for a first order approximation it will be assumed that they do not have any effect.

This gives a worst case situation that assumes each crossing wire is going to cause the maximum amount of impact to the victim wire. This is too pessimistic as it is unlikely that each aggressor wire will switch at exactly the right time to cause

perturbation. Therefore, a further processing phase is required to post-process these predictions.

The final phase looks at each aggressor wire and makes an attempt to classify how likely this wire is going to perturb the victim wire. A possible categorisation strategy might be:

**Very likely:** delay prediction indicates that the aggressor wire may toggle at the same time as the victim wire and that there are few other aggressor wires crossing this aggressor wire so it is fairly certain that it will switch at this time (assumptions are made to make it a first order approximation. Any more would make run times excessive).

**Possible:** delay prediction indicates that the aggressor wire may toggle at a time near to the victim wire, but the number of aggressor wires crossing this aggressor wire make it hard to predict exactly when it will switch.

**Unlikely:** Aggressor wire is on a net that cannot switch at a time where it will perturb the victim wire.

Once the categorisation has finished, these effects can be back-annotated onto the traditional static timing analysis as shown in figure 3. The degree of effect very likely...possible could be selected by the user to trade run times against accuracy.

As indicated in figure 3, the categorisation of the aggressor wires leads to the adding of additional margins 30 to the set-up time margin and the hold time critical region margin on either side of the rising edge of the clock pulse.

Referring now to the flow chart shown in figures 4, 5 and 6, figure 4 shows a general method of operation in accordance with the invention wherein in a first step 40, the various clocked paths in the integrated circuit are determined from a logic data base, each path being termed a signal path or victim net.

In step 42, the delay for a clock pulse passing through the signal path is determined, based on the characteristics of the signal path itself, without reference to external effects.

In step 44, a first signal path is selected, and in step 46 the wires (victim wires) forming the signal path are traced in a layout database of the integrated circuit and adjacent and crossing wires are determined, such wires being defined as aggressor wires.

In step 48, the amount of coupling for each adjacent wire is determined to the victim wires, based on an assumption that clocking occurs in the aggressor wire at the same time as in the victim wire.

In step 50, this procedure is repeated for each signal path in the data base.

In step 52, the aggressor nets are posted into categories for likelihood of affecting switching in the victim wire. In step 54, a timing analysis is carried out, as indicated above with reference to figure 2.

In step 56, the degree of accuracy for timing is selected, and in step 58 the static timing analysis results are modified to add margins based on the effects of aggressor nets in selected categories.

Step 52 is shown in more detail in figure 5. In step 60, it is determined whether in practice the aggressor net will switch at a different time to the victim wires. If the answer is YES, the aggressor wire is posted or flagged as "not likely" to effect the timing of the victim wires as at 62.

If the answer to determination at step 60 is NO, a further determination is made as to whether the aggressor net switches at a time close to the victim net, but because of the presence of other aggressor nets, it is not possible to make an accurate determination of delay prediction. If the answer to this determination is YES, then the aggressor wire is determined as "possible" as at 66, in that it may possibly effect the timing of the victim wires.

If the answer to the determination in step 64 is NO, then a further determination is made as to whether the aggressor net switches at a time close to the victim net, if the answer to this determination is YES, then the aggressor net is flagged or posted as in "likely", as at 70, to effect the timing of the victim net. If the answer to this determination is NO, then the aggressor net is posted as "not likely" to effect the timing of the victim net, as at 72.

This process is repeated for each aggressor net for any particular victim net, with the result that the aggressor nets are posted into three categories, "likely", "possible", or "not likely" to effect the timing of the victim net.

As shown in figure 6, steps 56 and 58 of figure 4 are shown in more detail in that margins are added to the clock timing of the victim wire in two selected ranges of accuracy. If as at 80, the analysis mode is set to pessimistic, and all significant effects on timing are to be taken into account, then an interval of time delta is added to the margins indicated in figure 3, as at 82, based on predicted perturbation from "likely" and "possible" data sets. If however the only the most significant perturbances are to be taken into account, i.e. a less accurate method of timing analysis, then as at 84, the analysis mode is set to normal, and as at 86 a time interval delta is added to the margins indicated in figure 3 based on the predicted perturbation from the "likely" data set, as determined in figure 5.

As indicated at 88, if no aggressor net perturbances are to be taken into account, then no timing interval is added to the margins of figure 3.

It will be understood that the predicted perturbation to be added to the timing interval will depend on the number of aggressor nets in the "likely" and "possible" data sets and thus the time interval to be added to the margin for timing will be extended based upon known statistical analysis methods. The effect of the number of aggressor nets would be scaled based on the topological and electrical nature of the coupling between two wires. For example, one aggressor wire that is driven by a strong source, such as a clock buffer running parallel a victim wire would have more effect than many aggressor wires running perpendicular to the victim wire (because the parallel wire will have a large coupling). This scaling can be calculated quite simply (for first order approximations), the coupling effect is capacitive and may formulae exist for calculating approximations for wires in different topological configurations.

The electrical impact can be calculated (again as a first order approximation) by using electrical circuit theory, the coupling capacitance and the knowledge of the signal's

propagation rate from the design tools' delay predictions that make the starting point for the static analysis algorithms.

It will be understood that the method illustrated in figure 4, 5 and 6 will be carried out on a computer system of the type used in analysis of integrated circuits and that the computer system will have modules added to it corresponding to the various method steps illustrated in figures 4, 5 and 6. Thus, the method disclosed in figures 4 to 6 is equivalent to the disclosure of the apparatus modules to be added to the computer system.

**Claims:**

1. A method of determining the timing for a synchronous integrated circuit, the circuit including a multiplicity of clocked elements interconnected by signal paths, the method comprising:
  - 1) Forming predictions for timing delays in said signal paths in the integrated circuit;
  - 2) Selecting a first such path, tracing wires in the integrated circuit forming the path (hereinafter referred to as victim wires) and determining adjacent and crossing wires thereto (hereinafter referred to as aggressor wires);
  - 3) For each aggressor wire, determining the amount of perturbation coupling to the victim wires of the first path;
  - 4) Dividing the aggressor wires into a plurality of categories depending on the clocked timing of the aggressor wires in relation to the clocked timing of the victim wires;
  - 5) Adding margins of error to the clocked timing of the victim wires independence upon the number of aggressor wires in one or more said categories.
2. A method according to claim 1, wherein step (3) is carried out taking into account one or more of the following factors:
  - a) whether the aggressor wire crosses or runs parallel to the victim wire;
  - b) the signal strengths in the victim and aggressor wires;
  - c) the layers in the integrated circuit which the wires are disposed;
  - d) operating conditions; and
  - e) the nature of aggressor wire
3. A method according to claim 1 or 2, wherein the aggressor wires are divided into three categories of likely, possible or unlikely to affect the timing of the victim wire.

4. A method according to claim 3, wherein the effect only of the likely category are taken into account.

5. A method according to claim 3, wherein the effect of the likely and possible categories are taken into account.

6. A method according to claim 3, wherein the effect of none of the categories is taken into account.

7. A method according to any of claims 3 to 6, wherein the effects of aggressor wires in any category are scaled according to their respective topological coupling and respective electrical signal coupling with the victim wire.

8. Apparatus for determining the timing of a synchronous integrated circuit, the circuit including a multiplicity of clocked elements interconnected by signal paths, the apparatus comprising:

1) Means for forming predictions for timing delays in said signal paths in the integrated circuit;

2) Means for selecting a first such path, tracing wires in the integrated circuit forming the path (hereinafter referred to as victim wires) and determining adjacent and crossing wires thereto (hereinafter referred to as aggressor wires);

3) Means for determining the amount of coupling, for each aggressor wire, to the victim wires of the first path;

4) Means for dividing the aggressor wires into a plurality of categories depending on the clocked timing of the aggressor wires in relation to the clocked timing of the victim wires;

5) Means for adding margins of error to the clocked timing of the victim wires independence upon the number of aggressor wires in one or more of said categories.

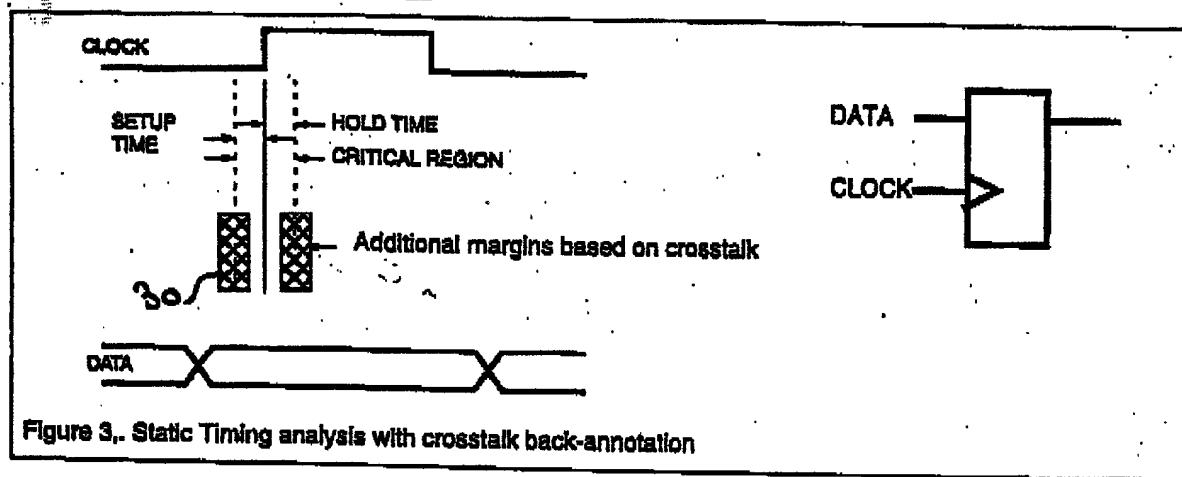
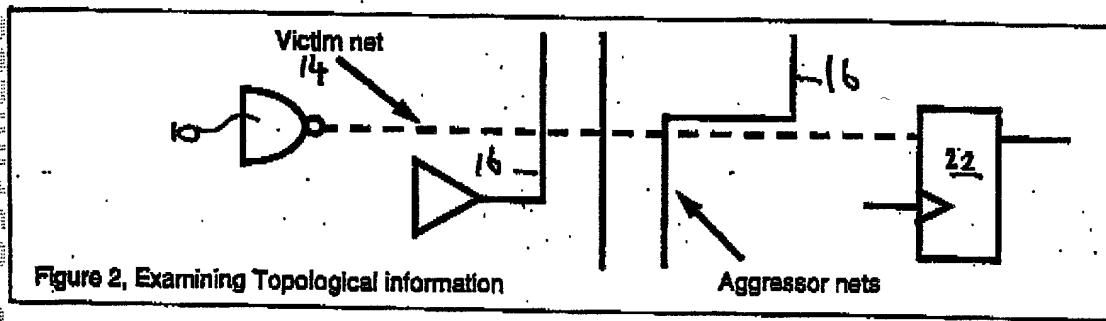
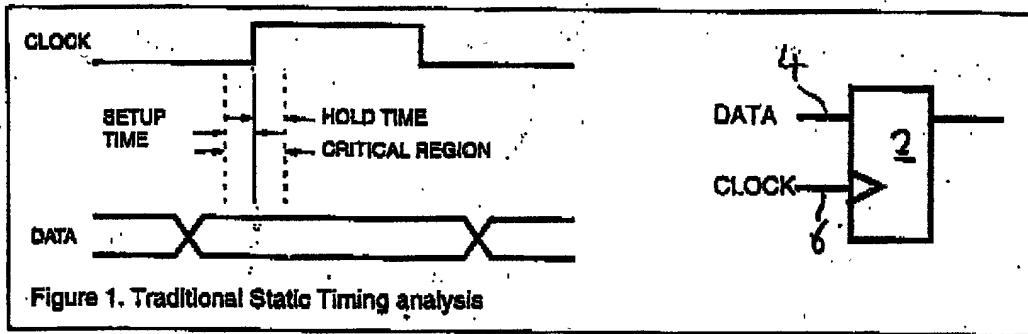
**ABSTRACT****DETERMINING TIMING OF INTEGRATED CIRCUITS**

A method of determining the timing of signal paths in a synchronous integrated circuit, taking into account the perturbing effect of switching in adjacent signal paths, the method comprising:

- 1) Forming predictions for timing delays in signal paths in the integrated circuit;
- 2) Selecting a first such path, tracing wires in the integrated circuit forming the path (victim wires) and determining adjacent and crossing wires thereto (aggressor wires);
- 3) For each aggressor wire, determining the amount of perturbation coupling to the victim wires of the first path;
- 4) Dividing the aggressor wires into a plurality of categories depending on the clocked timing of the aggressor wires in relation to the clocked timing of the victim wires;
- 5) Adding margins of error to the clocked timing of the victim wires in dependence upon the number of aggressor wires in one or more said categories.

Fig. 4

1 / 4



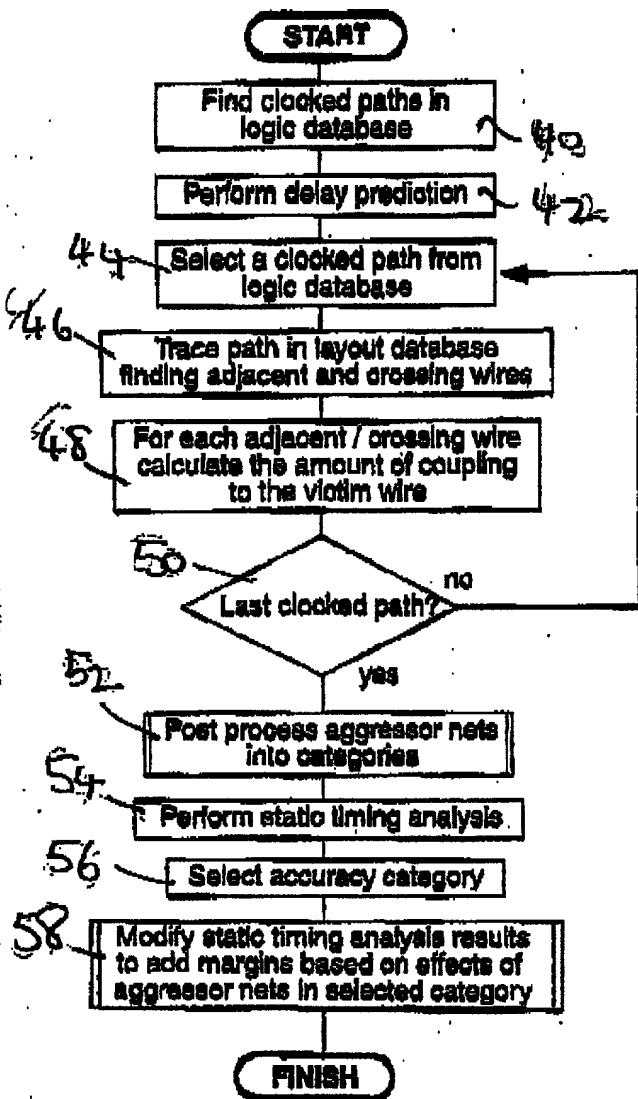
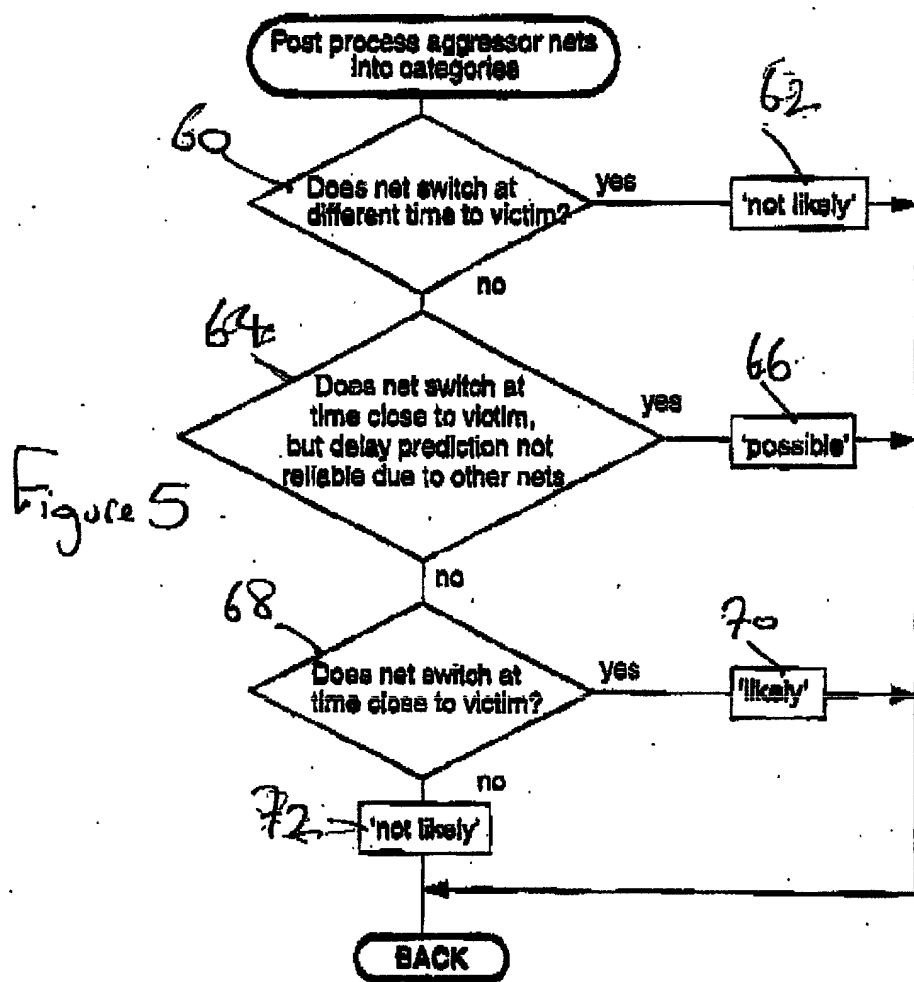
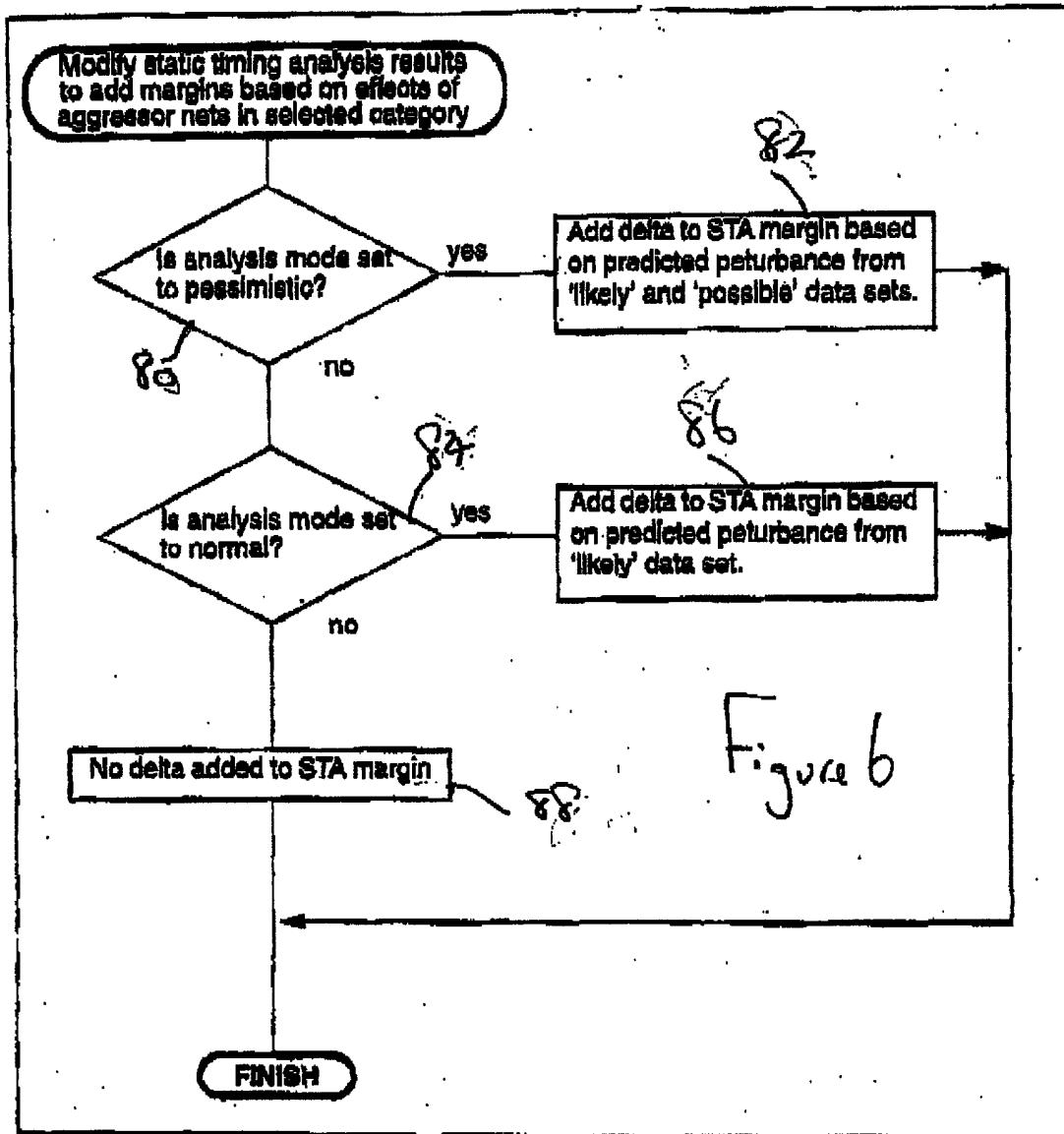


Figure 4

3/4



4/4



Docket No.  
30454-00230 (P-3376)

# Declaration and Power of Attorney For Patent Application

## English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

### DETERMINING TIMING OF INTEGRATED CIRCUITS

the specification of which

(check one)

is attached hereto.  
 was filed on \_\_\_\_\_ as United States Application No. or PCT International Application Number \_\_\_\_\_  
and was amended on \_\_\_\_\_  
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Priority Not Claimed

9814379.5

(Number)

GB

(Country)

2 July 1998

(Day/Month/Year Filed)

\_\_\_\_\_

(Number)

\_\_\_\_\_

(Country)

\_\_\_\_\_

(Day/Month/Year Filed)

\_\_\_\_\_

(Number)

\_\_\_\_\_

(Country)

\_\_\_\_\_

(Day/Month/Year Filed)

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

(Application Serial No.)

(Filing Date)

(Application Serial No.)

(Filing Date)

(Application Serial No.)

(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)

(Filing Date)

(Status)  
(patented, pending, abandoned)

(Application Serial No.)

(Filing Date)

(Status)  
(patented, pending, abandoned)

(Application Serial No.)

(Filing Date)

(Status)  
(patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (*list name and registration number*)

Steven E. Shapiro, Registration No. 35,676;  
 Joseph G. Swan, Registration No. 41,338;  
 D. James Chung, Registration No. 41,678; and  
 Howard H. Seo, Registration No. 43,106

of the firm of Mitchell, Silberberg & Knupp LLP  
 11377 West Olympic Boulevard  
 Los Angeles, CA 90064  
 (310) 312-2000

And I/We hereby further appoint:

David G. Pursel, Registration No. 28,659;  
 Bruce Hopenfeld, Registration No. 39,714;  
 Ralph R. Veseli, Registration No. 33,807;  
 David Lucente, Registration No. 36,202; and  
 Sandeep Jaggi, Registration No. 43,331

whose address is:  
 LSI Logic Corporation  
 1551 McCarthy Boulevard  
 Milpitas, CA 95035  
 (408) 433-8000

Send Correspondence to: **Steven E. Shapiro, Esq.**  
**MITCHELL, SILBERBERG & KNUPP LLP**  
**11377 West Olympic Boulevard**  
**Los Angeles, California 90064**

Direct Telephone Calls to: (*name and telephone number*)  
**Steven E. Shapiro, Telephone Number (310) 312-2000, Facsimile Number (310) 312-3100**

Full name of sole or first inventor <b>William Eric Corr</b>	Date
Sole or first inventor's signature	
Residence <b>Twickenham, Mid, England</b>	
Citizenship <b>British</b>	
Post Office Address <b>12 Knowe Road, Twickenham, Mid, England TW2-6QH United Kingdom</b>	

Full name of second inventor, if any	
Second inventor's signature	Date
Residence	
Citizenship	
Post Office Address	